

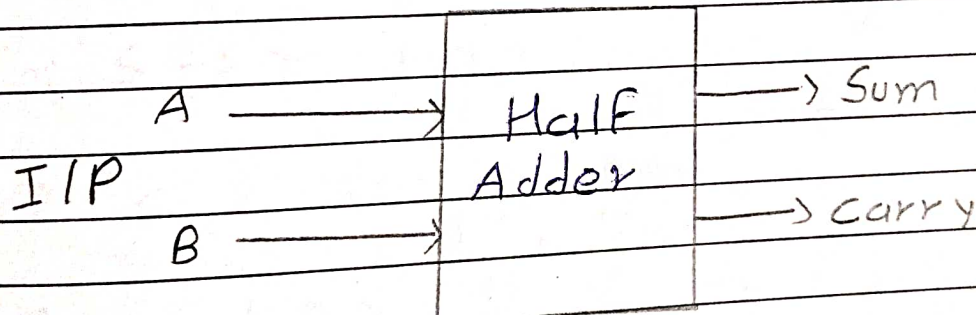
* Half Adder:

Half Adder circuit has two input and two output.

Half Adder circuit use to add two input digits.

Half Adder circuit Generates carry and sum.

- Block Diagram:



- Half adder is a combinational logic circuit which is designed by one Ex-OR gate and one AND gate.

Half adder Generates two input digits sum and carry

- Truth Table:

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

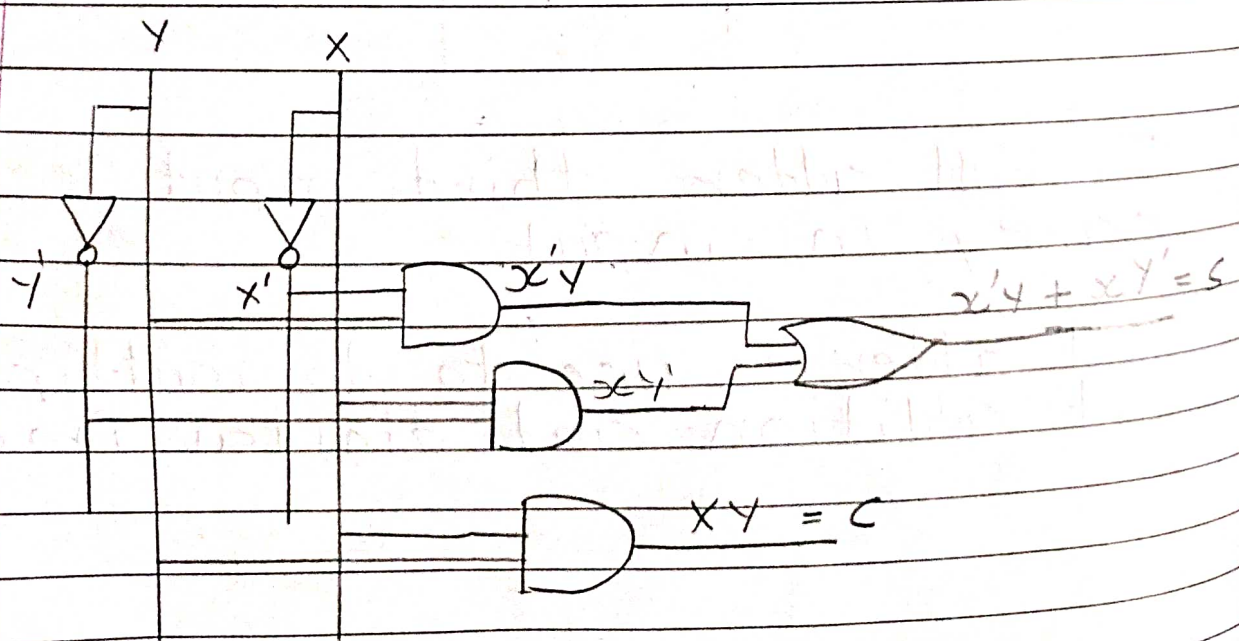
From the table,

IF $A = 0$ then $S = 0$ and
 $A = 1$ then $S = 1$ and
 $A = 1, B = 1$ then $C = 1$.

$$S = x'y + xy'$$

$$C = xy$$

- Circuit Diagram



- Advantages :

Half adder has simple design and easy to build.

- Disadvantages :

Half adder does not take care the previous carry for addition.

- Application:

- 1 This circuit used in Computer.
- 2 Used for build various digital measuring instruments.
- 3 Used in calculators.

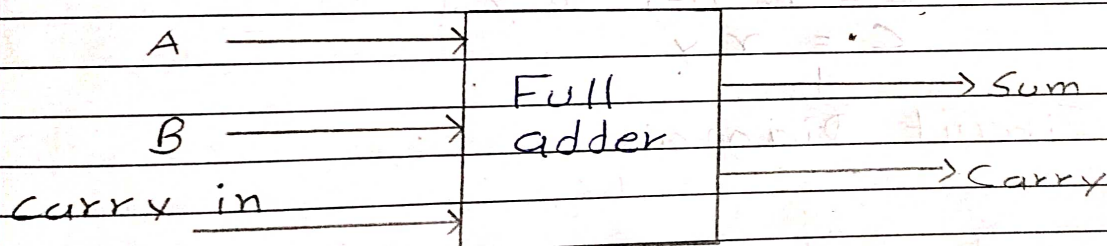
* Full adder:

Full adder circuit has three input and two output.

A Full adder is a combinational circuit that perform arithmetic sum of three input bits.

Full adder circuit Generates carry and sum.

- Block Diagram:



In Full adder, third input is a carry in input.

Full adder is use to do multiple bit addition and digital Processors.

- Truth table:

X	Y	Z	S	C
0	0	0	0	0
0	0	1	①	0
0	1	0	①	0
0	1	1	0	1 ✓
1	0	0	①	0
1	0	1	0	1 ✓
1	1	0	0	1 ✓
1	1	1	①	1 ✓

K-map For - S

	00	01	11	10
0	0	1	3	2
1	1	3	2	0

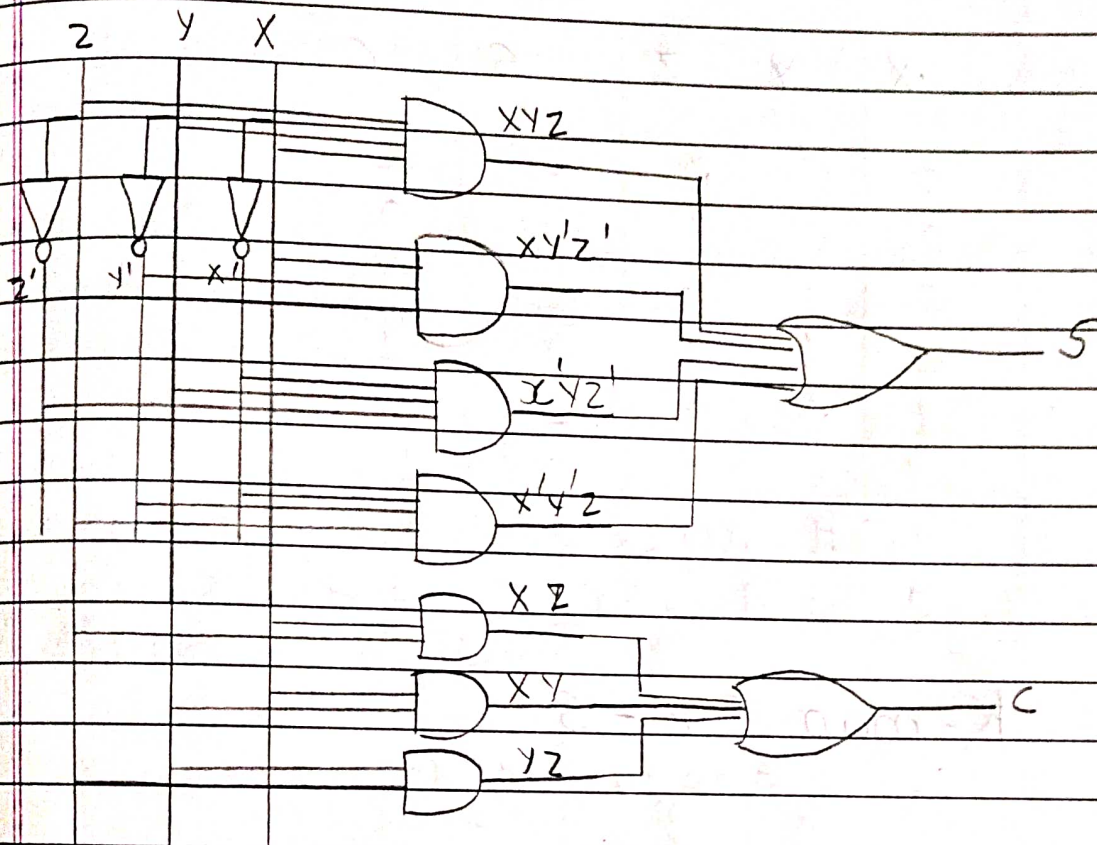
$$S = x'y'z + x'y'z' + xy'z' + x'yz$$

K-map For - C

	00	01	11	10
0	0	1	3	2
1	1	①	①	①

$$C = xz + xy + yz$$

- Circuit Diagram:



- Advantages:

Full adder has the ability to perform the three bits addition.

- Disadvantages:

It is not suitable for multiple bit addition.

- Application:

1. build varieties of calculator

2 Use For ALU in computer.

3 Used For ripple counter.

* Binary Parallel Adder:

Binary Parallel Adder is a digital circuit that produces the arithmetic sum of two binary number.

In Binary Parallel Adder, Full adders are connected in a chain.

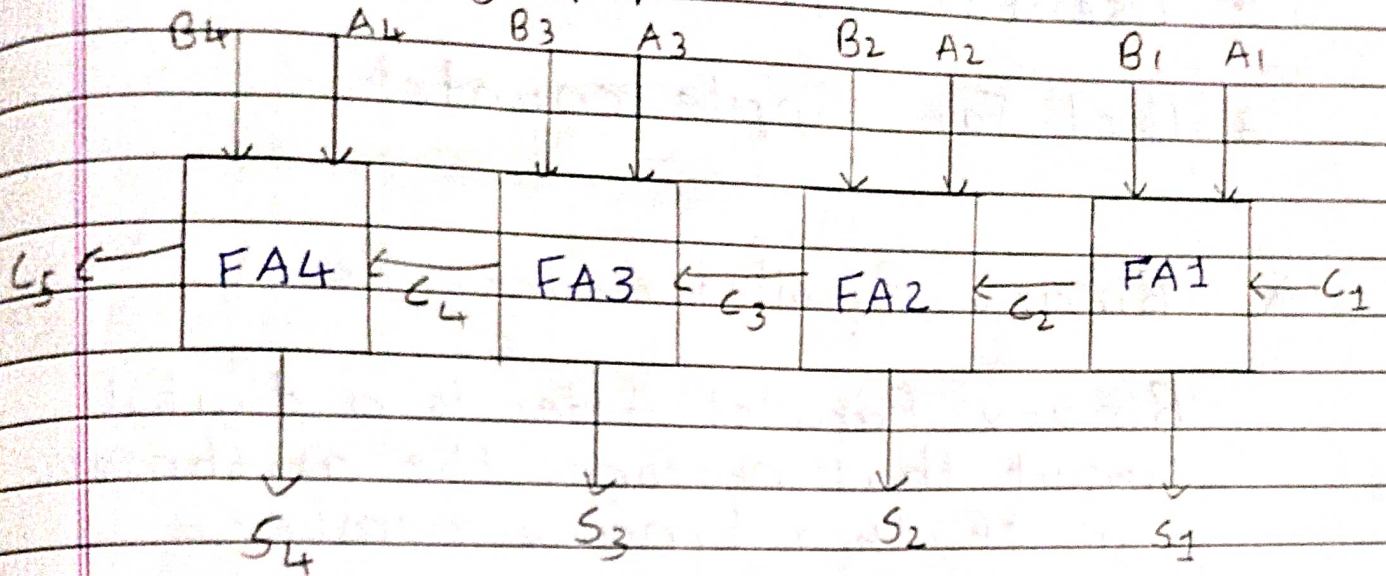
First adder output carry is connected with each full adder to the input carry of the next adder.

Binary Parallel adder is use to find sum of two Binary number that is greater than one bit.

N-bit Parallel adder requires a n-bit Full adder to perform the operation.

Binary Parallel adder performs the addition operation faster as compared to single adder.

- Block Diagram:



This a block Diagram of 4-Bit Binary Parallel adder.

- Advantages:

The Binary Parallel adder performs the addition operation faster as compared to single adder.

- Disadvantages:

In Binary Parallel adder, each full adder has to wait for the carry which is generated by previous full adder in chain.

- Application :

Binary Parallel adder is use to Finding the sum of two binary number that is greater than one bit.

* Decimal Adder :

Decimal adder is called BCD adder. BCD stands for binary coded Decimal.

Decimal Adder is used to perform the addition of BCD numbers.

Decimal adder vary from 0 to 9 numbers.

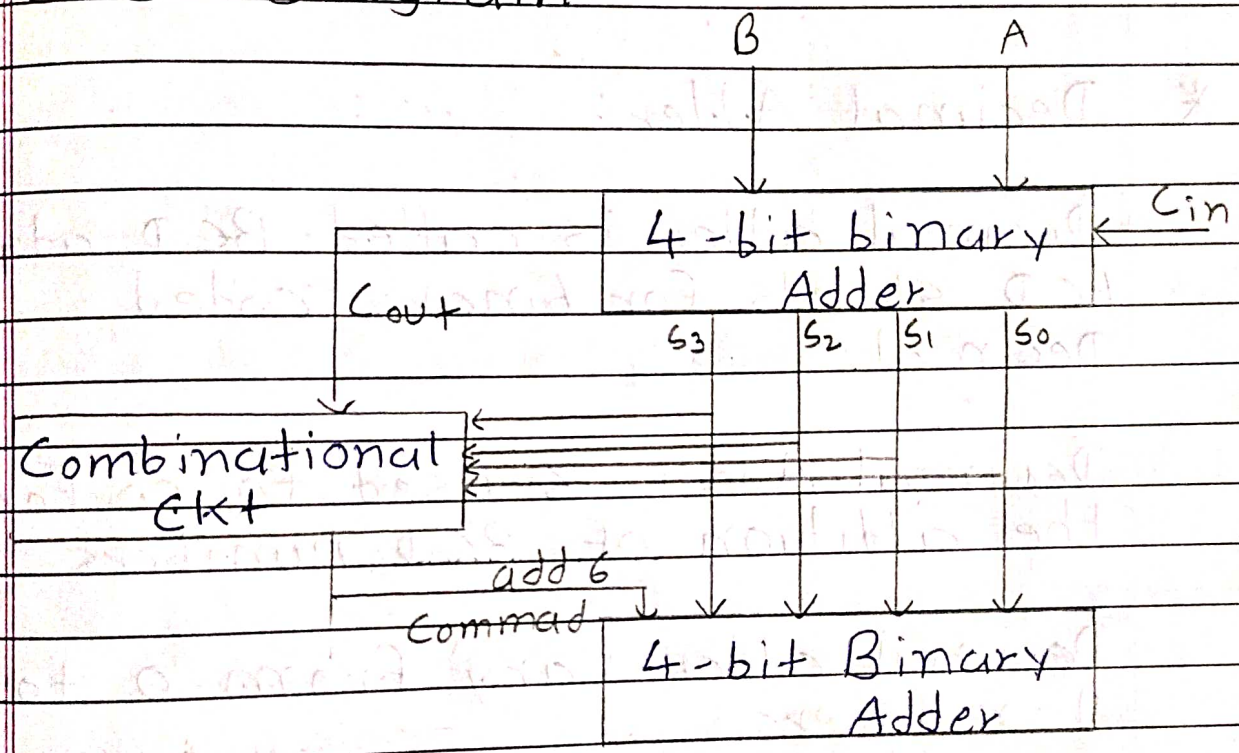
If number is not in 0 to 9 range, then we have to convert number into the Decimal.

For convert the number into the Decimal, we have to add 6 into the number.

Ex. $1011 = 11 \rightarrow$ This is not Decimal

$$\begin{array}{r}
 \therefore \quad 1011 \quad \text{add } 6 \text{ (0110)} \\
 + 0110 \\
 \hline
 \underline{10001} \\
 1 \quad 1
 \end{array}$$

- Block Diagram:



In Decimal adder, we have to use 4-bit Binary adder.

In Decimal Adder, we can use Combinational ckt.

Using Combinational ckt we can add the two number.

Truth table:

I/P				O/P
S ₃	S ₂	S ₁	S ₀	
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Ans. in

BCD Form

Ans. will add by 6

For, Finding the Combinational ckt, we have to draw k-map using truth table.

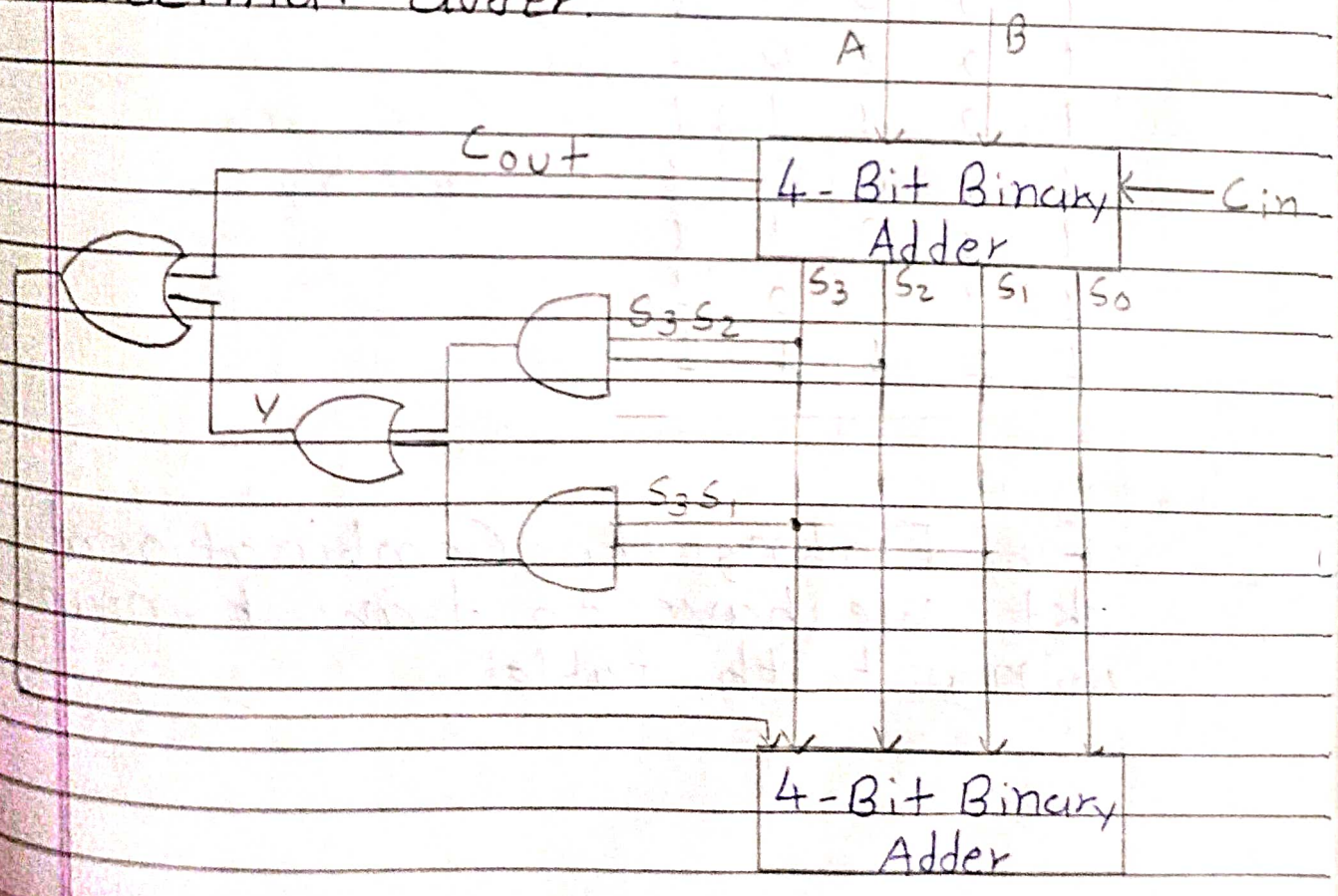
- K-map of ckt:

	$S_1 S_0$			
$S_3 S_2$	0	1	3	2
	4	5	7	6
	12	13	15	14
	8	9	11	10

(Note: The K-map shows 1s in cells (12,13), (13,14), (15,14), (15,11), (11,10), and (10,10).)

$$Y = S_3 S_2 + S_3 S_1$$

- Combinational Ckt Diagram: with Decimal adder.



- Advantages:

BCD adder allows easy conversion between decimal base-10.

- Disadvantages:

BCD adder have different rules for addition.

- Application:

- 1 Used in the computer
- 2 Used in calculator to performs arithmetic operation.

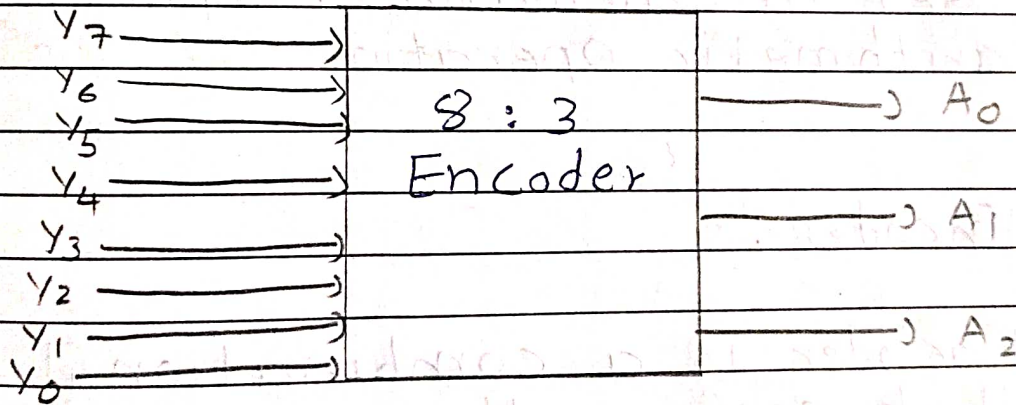
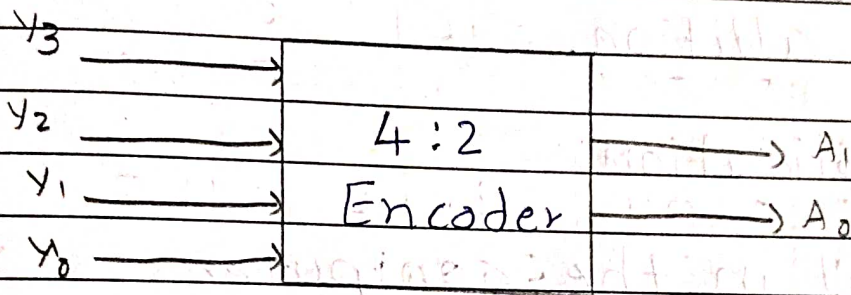
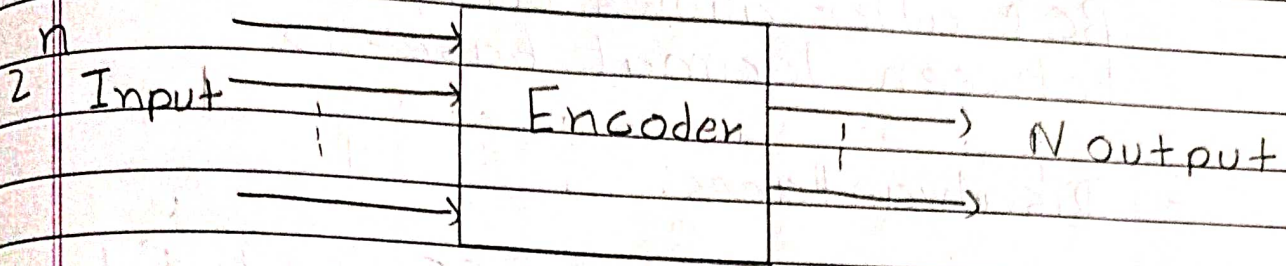
* Encoder:

Encoder is a combinational ckt that perform the reverse operation of decoder.

Encoder has 2^n input line and n output line.

IF encoder has 2^3 input line then 3 is a output line.

- Block Diagram:



In 4:2 Encoder, 4 Input line and 2 Output line.

In 8:3 Encoder, 8 Input line and 3 Output line.

- Truth table of 8:3 Encoder:

IIP								OIP		
Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0	A_2	A_1	A_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

$$A_0 = Y_7 + Y_5 + Y_3 + Y_1$$

$$A_1 = Y_7 + Y_6 + Y_3 + Y_2$$

$$A_2 = Y_7 + Y_6 + Y_5 + Y_4$$

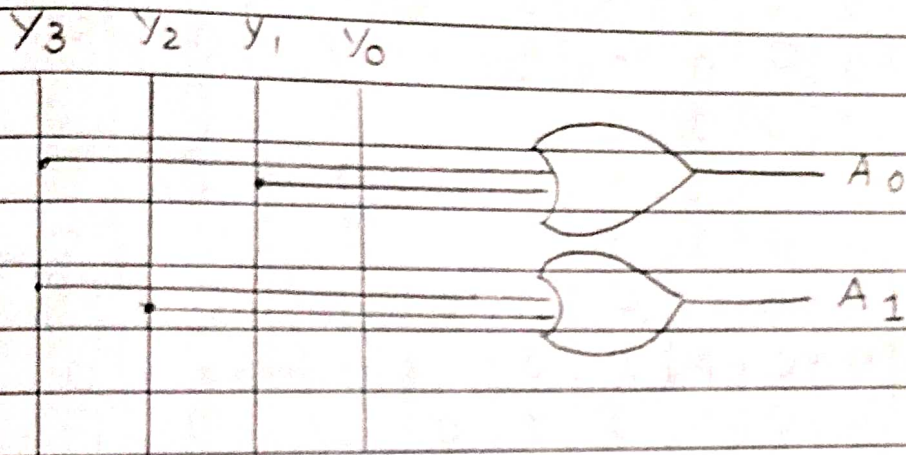
- Truth table of 4:2 Encoder:

IIP				OIP	
Y_3	Y_2	Y_1	Y_0	A_1	A_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

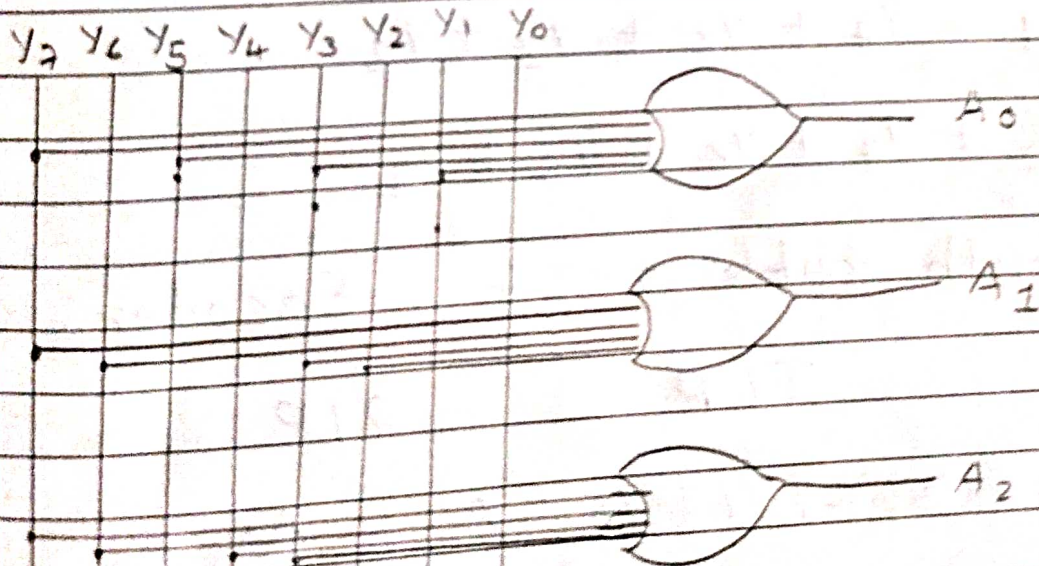
$$A_0 = Y_3 + Y_1$$

$$A_1 = Y_3 + Y_2$$

- CKT Diagram for 4:2 Encoder:



- CKT Diagram for 8:3 Encoder:



- Advantages:

Encoder is reduce time and Reduce cost.

- Disadvantages:

Encoder is subject of magnetic radio interference.

- Application.

1 Encoder is use in automatic health monitoring system.

2 Used in home automation System.

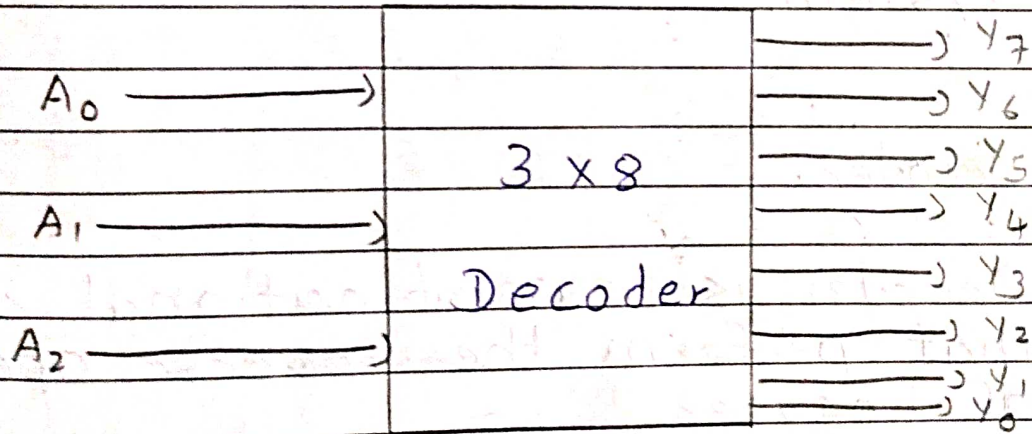
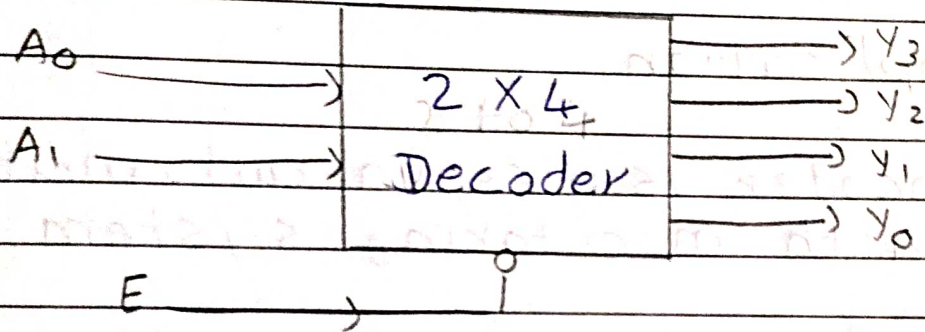
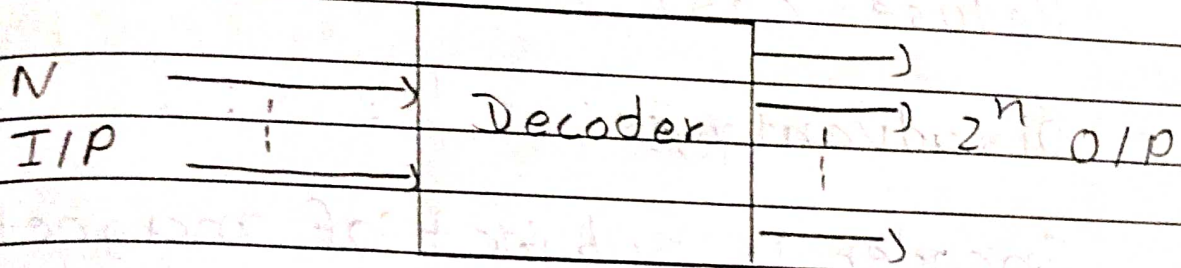
* Decoder:

Decoder is a combinational ckt that perform the reverse operation of Encoder.

Decoder has n input line and 2^n output line.

If Decoder has 3 input line, then 8 output line.

- Block Diagram:



In 2×4 Decoder, 2 input line and 4 output line.

In 3×8 Decoder, 3 input line and 8 output line.

- Truth table For 2x4 Decoder:

I/P			O/P			
E	A	B	D ₀	D ₁	D ₂	D ₃
1	1	1	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

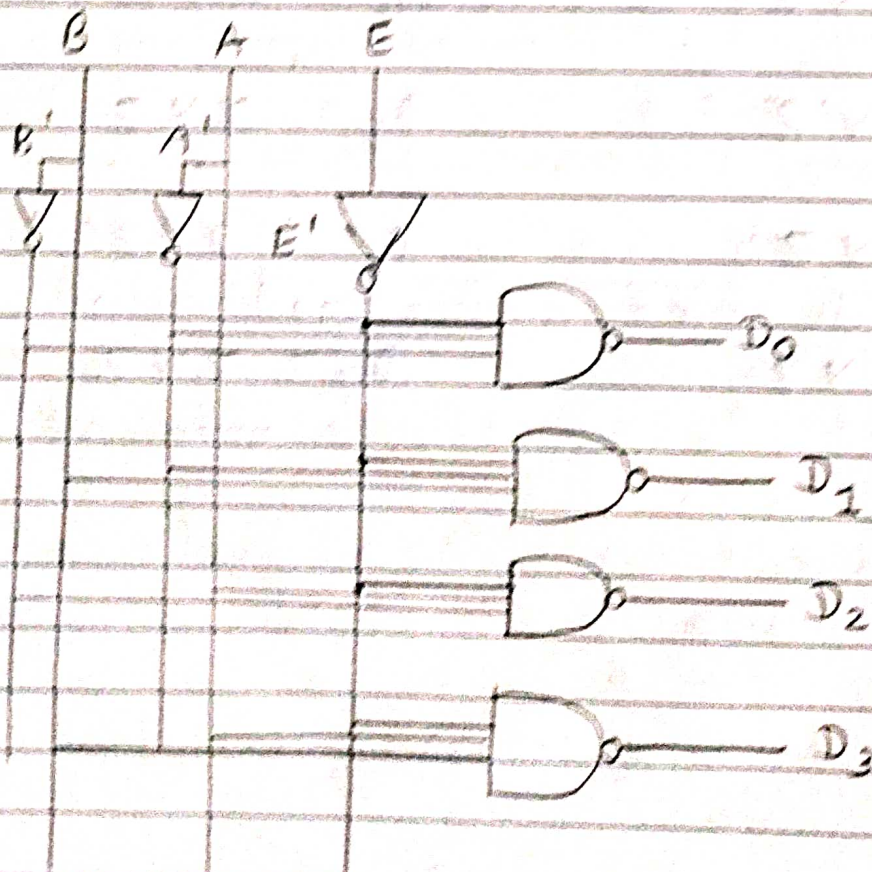
$$D_0 = E'A'B'$$

$$D_2 = E'AB'$$

$$D_1 = E'A'B$$

$$D_3 = E'AB$$

- CKT Diagram For 2x4 Decoder:



- Truth table For 3x8 Decoder:

I/P			O/P							
X	Y	Z	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

$$D_0 = x'y'z'$$

$$D_4 = xy'z'$$

$$D_1 = x'y'z$$

$$D_5 = xy'z$$

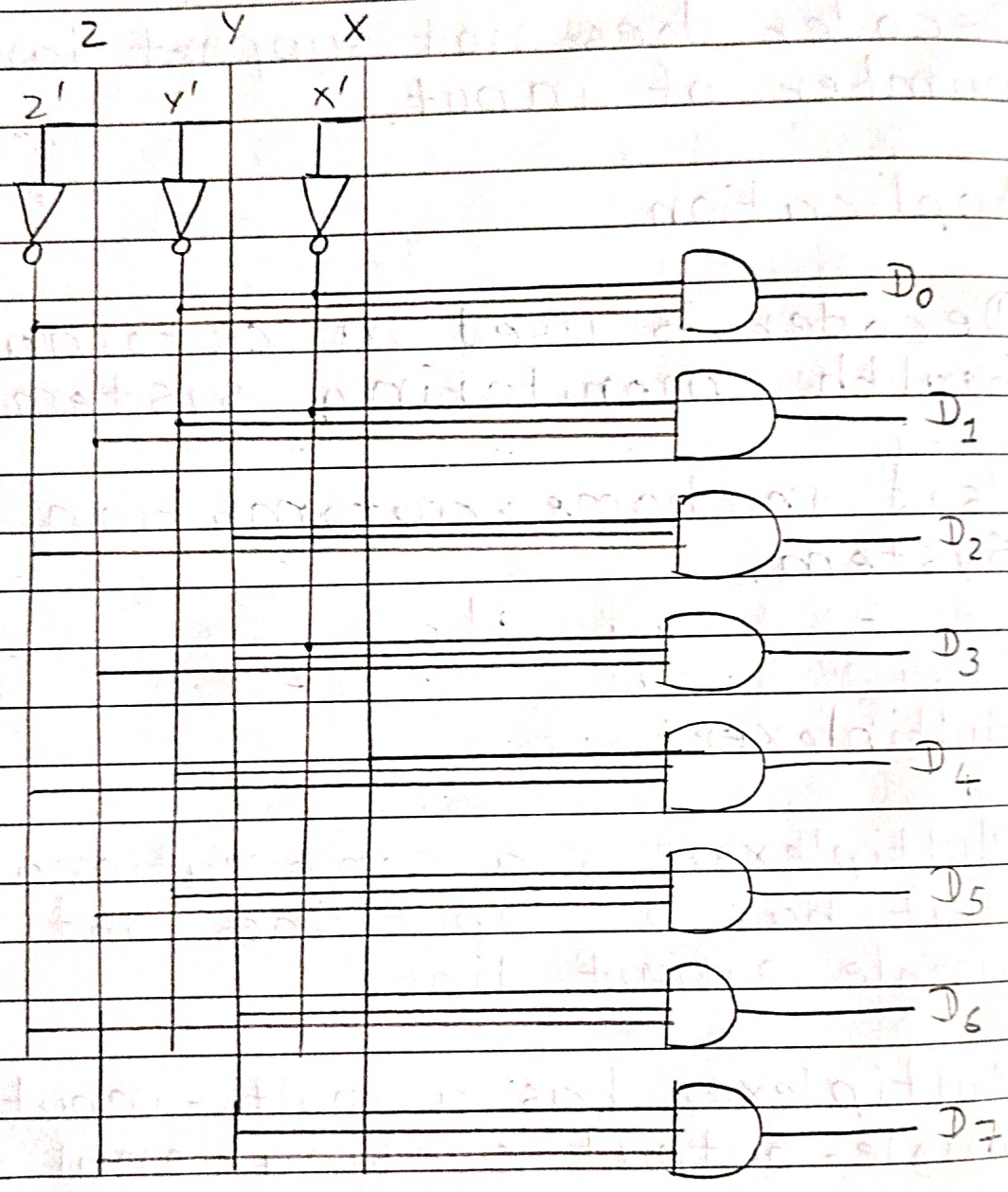
$$D_2 = x'yz'$$

$$D_6 = xyz'$$

$$D_3 = x'yz$$

$$D_7 = xyz$$

- Ckt Diagram For 3x8 Decoder



- Advantages:

Decoder is Reduse time and reduse cost.

- Disadvantages:

Decoder does not support larger number of input.

- Application.

1 Decoder is used in automatic health monitoring system.

2 Used in home automation system.

* Multiplexer:

Multiplexer is a combinational ckt that has 2^n input lines and a single output line.

Multiplexer has a multi-input and single-output combinational ckt.

In Multiplexer there are selection line is also use.

If we have 2×1 Mux, then we have 2 input line, 1 selection line and one output line.

IF we have 4×1 Mux, then we have 4 input line, 1 output line and 2 selection line.

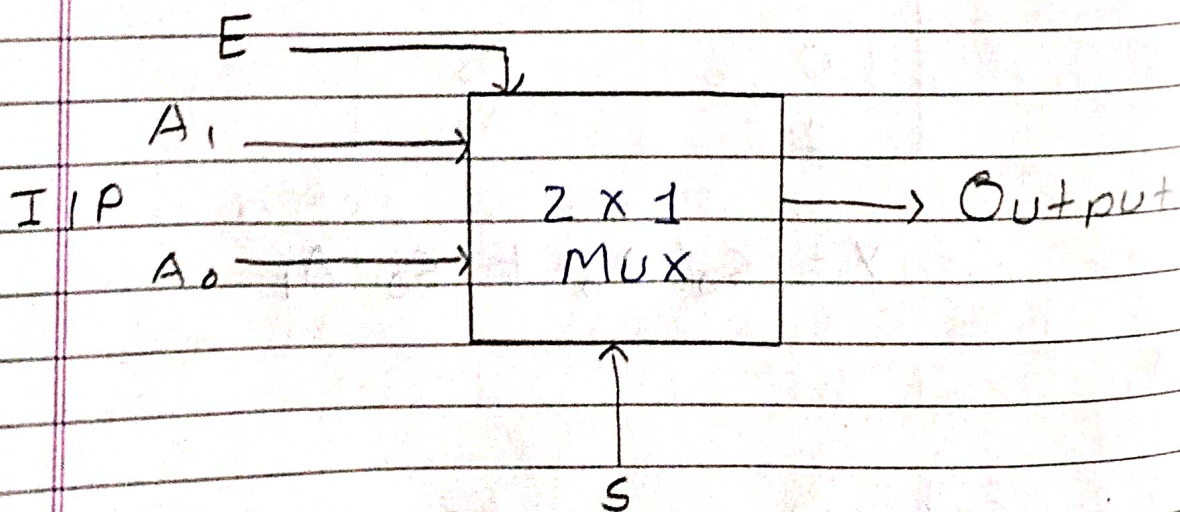
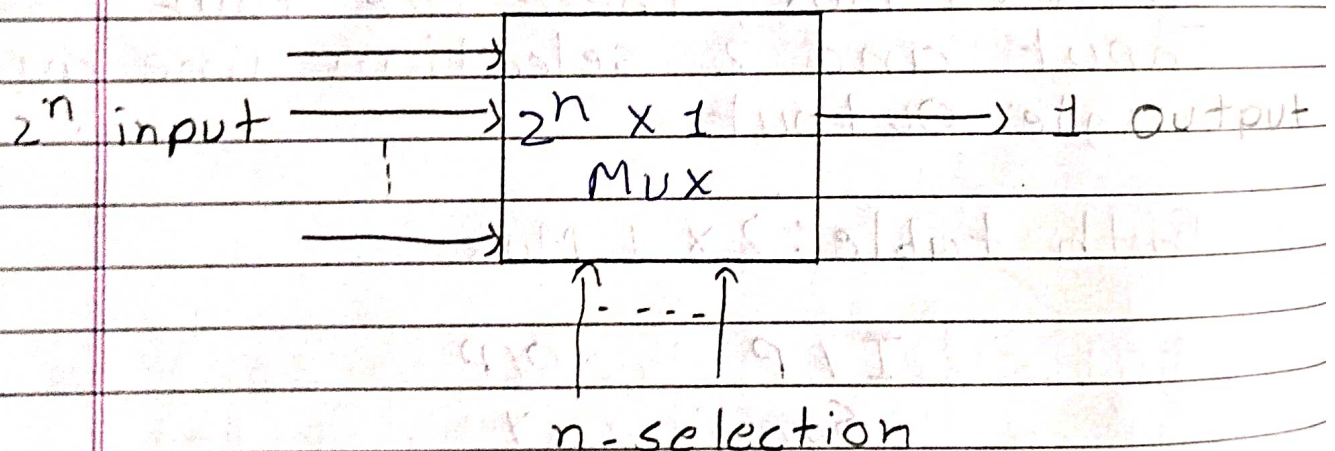
IF we have $2^n \times 1$ MUX,
then

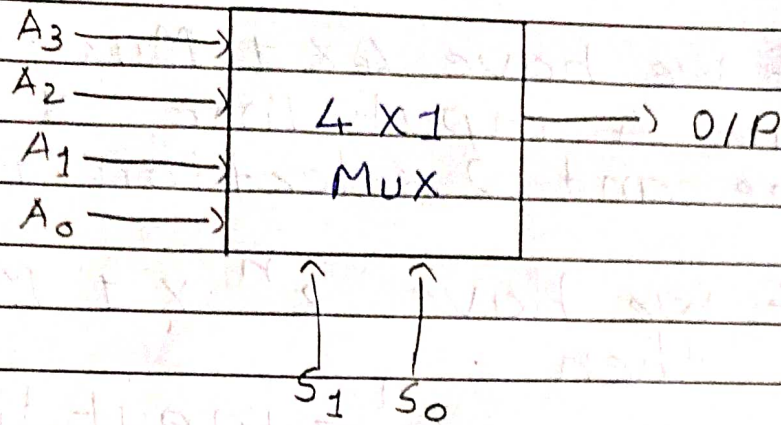
2^n - input line

1 - Output line

n - selection line.

- Block Diagram:





In 2×1 Mux, there are only two input A_0 and A_1 , 1 selection line and single output.

In 4×1 Mux there are four input and 2 selection line and single output.

→ Truth table: 2×1 Mux

I/P	O/P
S_0	Y
0	A_0
1	A_1

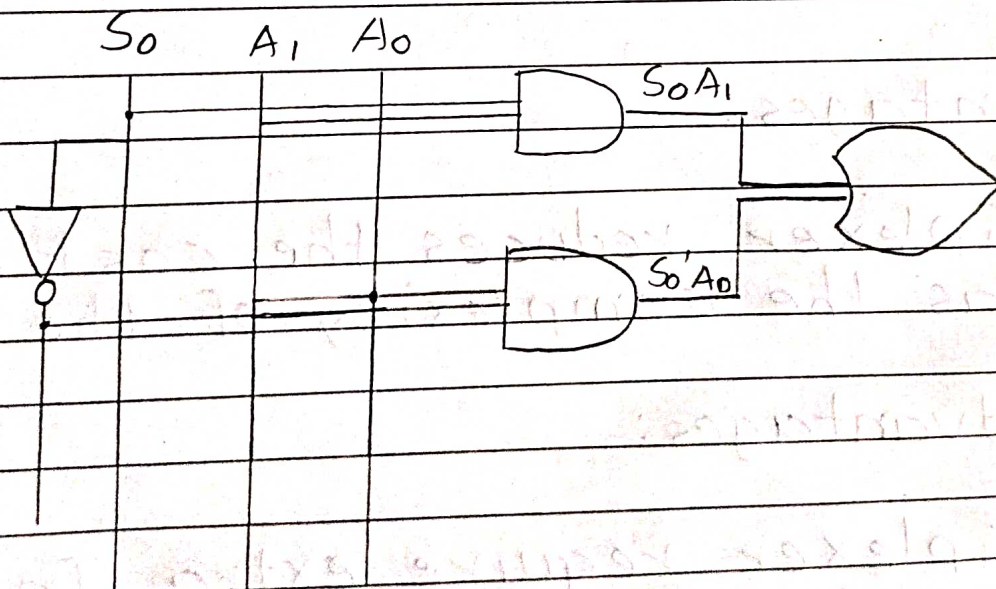
$$\therefore Y = S_0' A_0 + S_0 \cdot A_1$$

- 4x1 Mux:

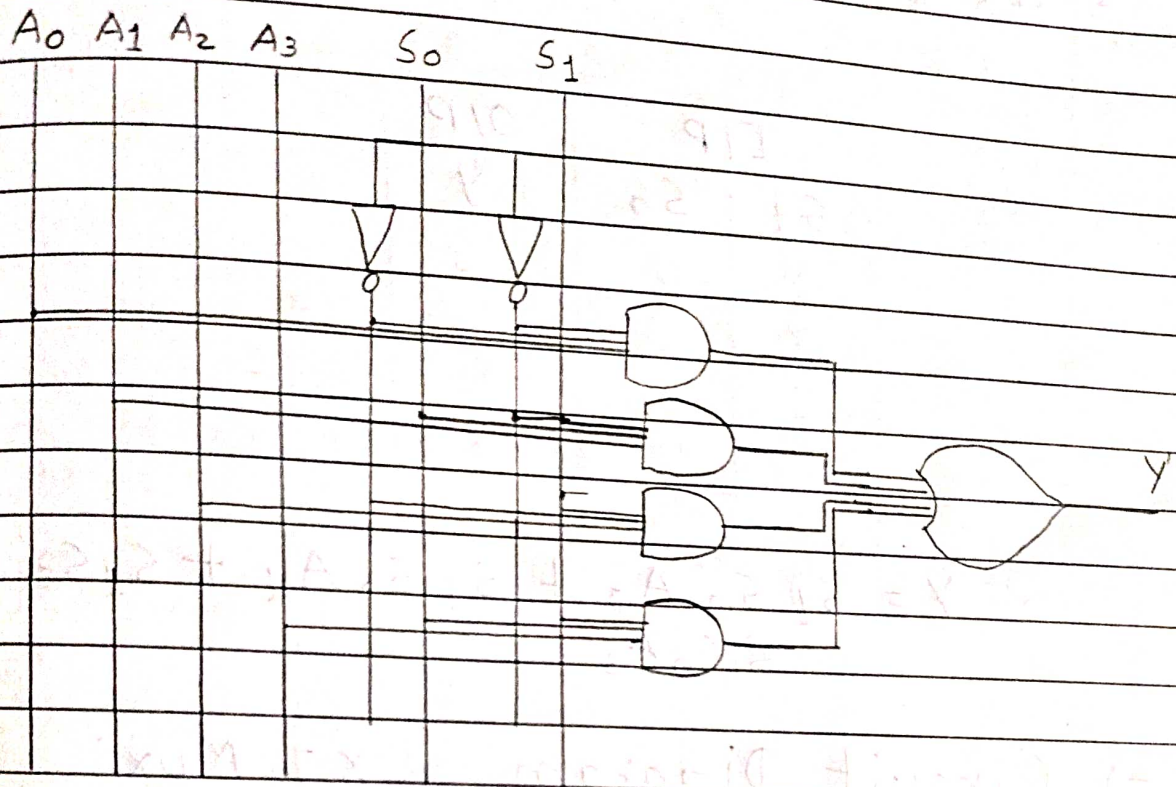
IIP		OIP
S_1	S_0	Y
0	0	A_0
0	1	A_1
1	0	A_2
1	1	A_3

$$\therefore Y = S_1' S_0' A_0 + S_1' S_0 A_1 + S_1 S_0' A_2 + S_1 S_0 A_3$$

-> Circuit Diagram: 2x1 Mux:



- 4 X 1 Mux :



- Advantages:

Multiplexer reduces the cost as well as the complexity of the circuit.

- Disadvantages:

Multiplexer require extra Input for control multiplexer.

- Application:

1 It used in computer memory.

2 Multiplexer is also used in communication system.

3 Multiplexer is also used in Telephone network.

* De-multiplexer:

De-multiplexer is a combinational ckt that has single input line and 2^n output line.

De-multiplexer has a multi output and single input line.

In De-multiplexer there are selection line is also use.

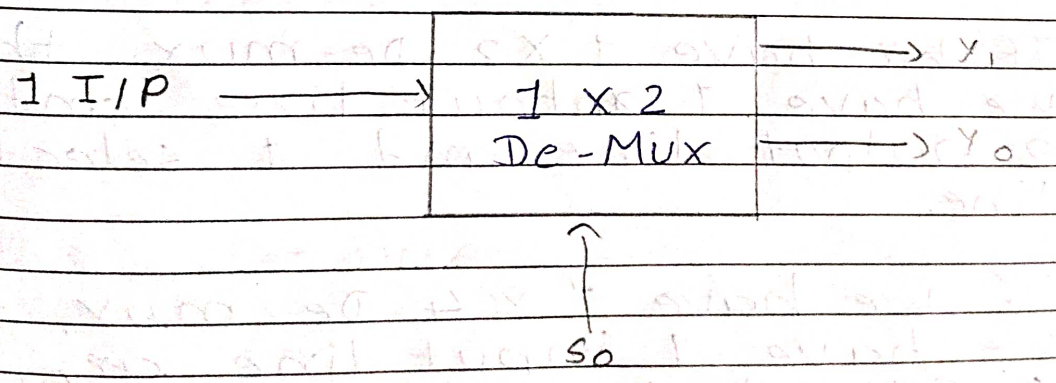
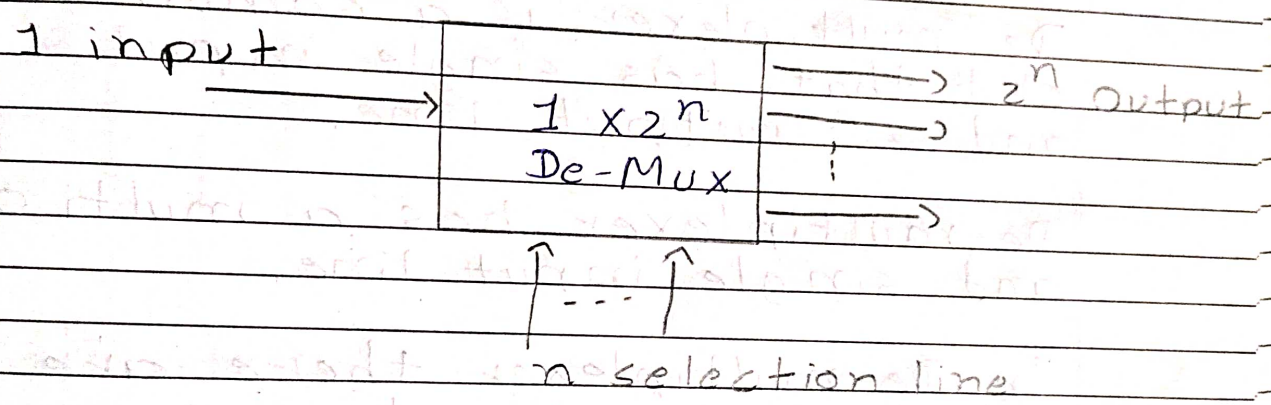
If we have 1×2 De-mux, then we have 1 input line and 2 output line and 1 selection line.

If we have 1×4 De-mux, then we have 1 input line or, 4 output line and 2 selection line.

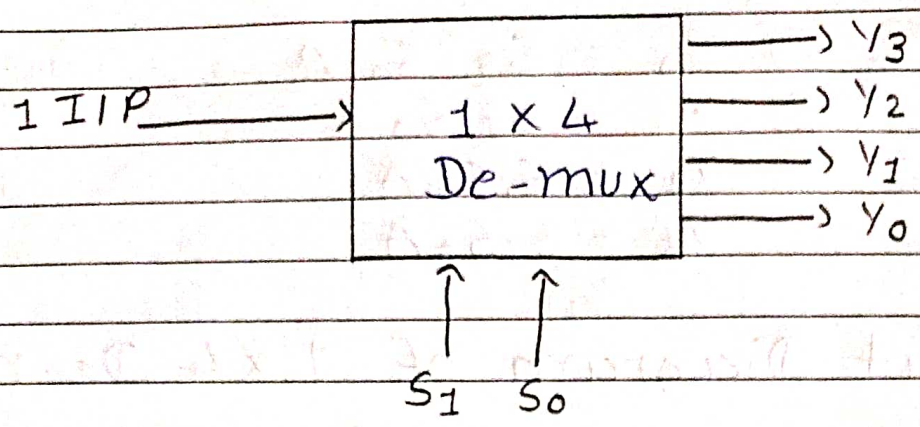
If we have 1×2^n De-mux,

- 1 input line
- 2^n output line
- n selection line.

- Block Diagram:



In 1×2 De-Mux, there are only one input and 2 output Y_1 and Y_0 .



In 1 x 4 De-mux, there are One input, 4 output line and 2 selection line

- Truth table: 1 x 2 De-mux

I/P	O/P	
S ₀	Y ₁	Y ₀
0	0	A
1	A	0

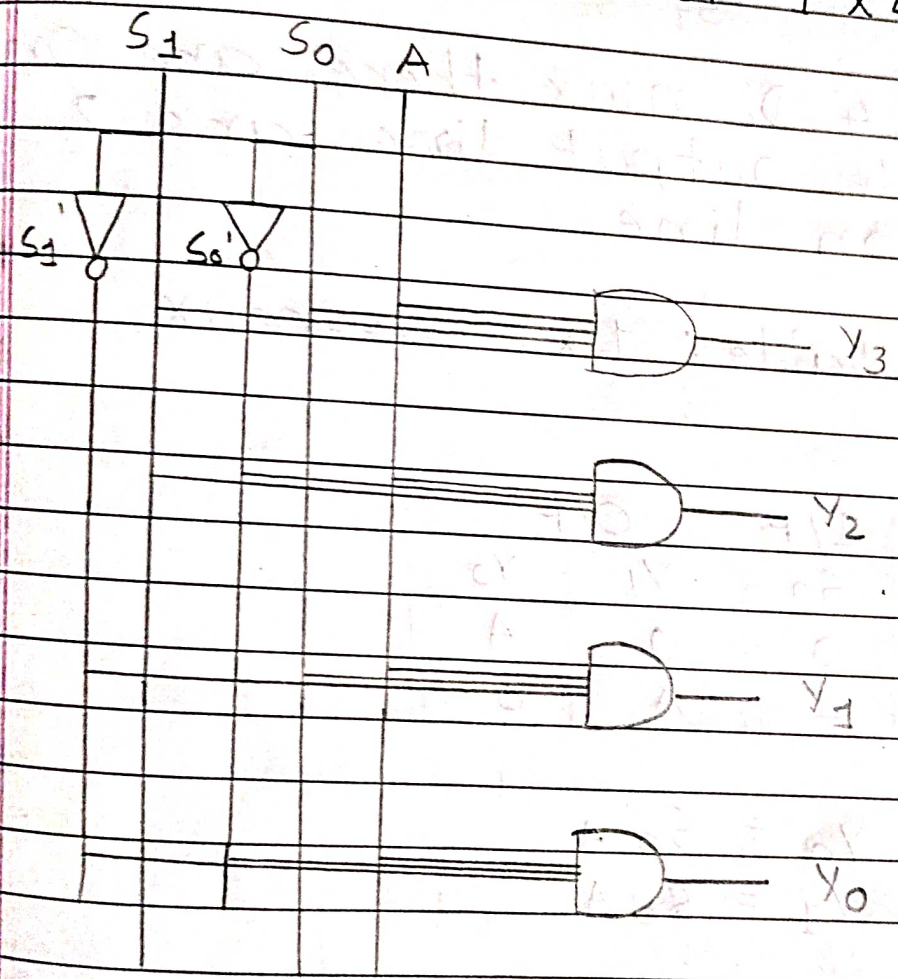
∴ $Y_0 = S_0' A$
 ∴ $Y_1 = S_0 A$

- 1 x 4 De-mux

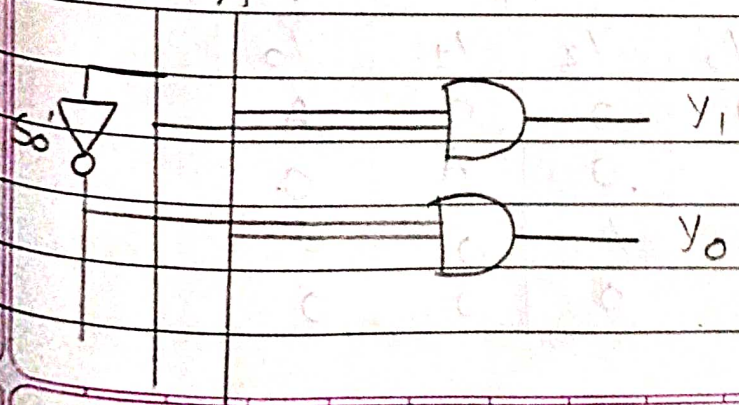
I/P		O/P			
S ₁	S ₀	Y ₃	Y ₂	Y ₁	Y ₀
0	0	0	0	0	A
0	1	0	0	A	0
1	0	0	A	0	0
1	1	A	0	0	0

$$\begin{aligned} \therefore Y_0 &= S_1' S_0' A \\ \therefore Y_1 &= S_1' S_0 A \\ \therefore Y_2 &= S_1 S_0' A \\ \therefore Y_3 &= S_1 S_0 A \end{aligned}$$

→ Circuit Diagram of 1 x 4 De-mux:



1 x 2 De-mux
S0 A



- Advantages:

De-Multiplexer reduces the cost as well as the complexity of the circuit.

- Disadvantages:

De-Multiplexer, might delays a single.

- Application:

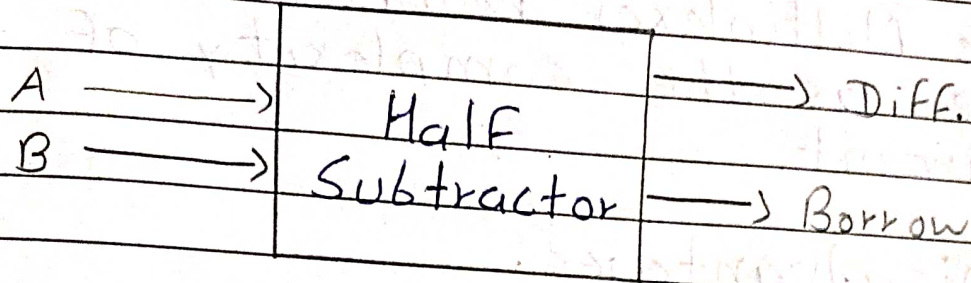
- 1 De-multiplexer is used in communication system.
- 2 De-multiplexer is used in clock data recovery solutions.

* Half Subtractor:

Half Subtractor is a combination ckt with two input and two output which is difference and borrow.

Half Subtractor Gives difference between to binary bit.

- Block Diagram:



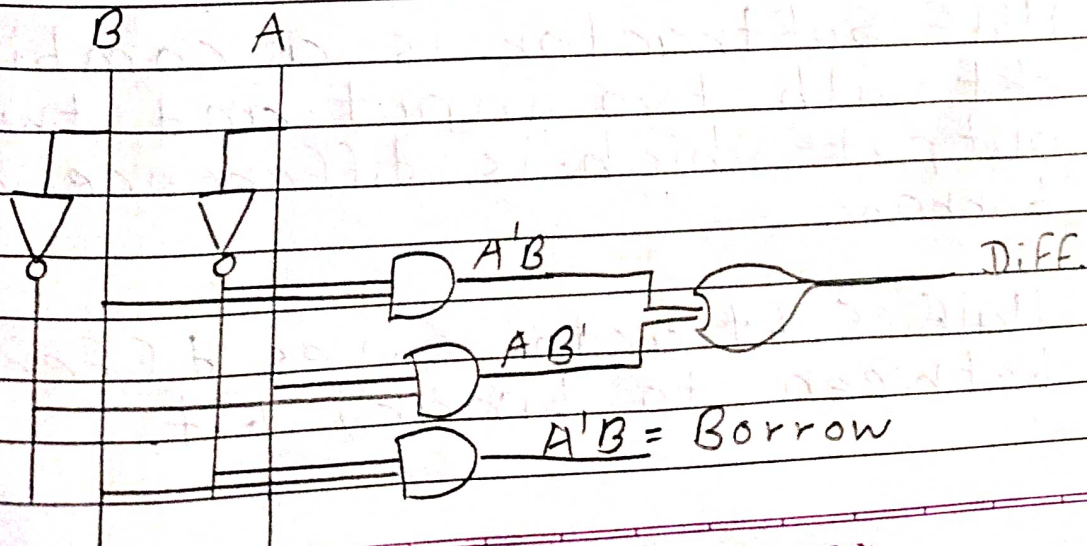
- Truth table:

A	B	DIFF.	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

$$\text{DIFF.} = A'B + AB'$$

$$B = A'B$$

- Circuit Diagram:



- Advantages:

Half Subtractor has the ability to perform the subtraction within two bits.

- Disadvantages:

Half Subtractor does not take care of previous borrow.

- Application:

- 1 Half Subtractor used in ALU.
- 2 Half Subtractor used to reduce the force of radio signals.

* Full Subtractor:

A	B	C	D	B
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

$$\begin{aligned}
 \rightarrow D &= \underline{A'B'C} + A'BC' + AB'C' + \underline{ABC} \\
 &= C(A'B' + AB) + C'(A'B + AB') \\
 &= C(A \oplus B)' + C'(A \oplus B) \\
 &\quad \quad \quad (X) \\
 &= CX' + C'X = X \oplus C
 \end{aligned}$$

$$D = A \oplus B \oplus C$$

$$\begin{aligned}
 \rightarrow C &= \underline{A'B'C} + A'BC' + A'BC + \underline{ABC} \\
 &= C(CAB + A'B') + A'BC(C + C') \\
 &= C(A \oplus B)' + A'B
 \end{aligned}$$

→ Difference Diagram:

